AMENDMENTS TO THE CLAIMS

1. (Currently amended) A DMA controller comprising:

a DMA datapath for transferring data from a DMA source to a DMA destination; and

channel control logic for controlling transfer of data through the DMA datapath in response to parameters contained in at least one DMA descriptor having a programmable format, wherein each DMA descriptor defines a single DMA transfer, wherein the DMA descriptor includes a next descriptor pointer that points to a next descriptor in a descriptor list, wherein the next descriptor pointer is selected from (1) none, which indicates descriptor array mode, (2) half of the next descriptor pointer, which indicates small descriptor list mode, and (3) all of the next descriptor pointer, which indicates large descriptor list mode, and wherein the DMA descriptor further includes a flow mode that defines a next operation selected from an autobuffer mode, the descriptor array mode, the small descriptor list mode and the large descriptor list mode.

2. (Original) A DMA controller as defined in claim 1, wherein the DMA descriptor has a programmable size.

3. (Original) A DMA controller as defined in claim 1, wherein the DMA descriptor has a programmable operating mode.

4. (Cancelled)

5. (Original) A DMA controller as defined in claim 1, wherein the DMA descriptor includes a next descriptor size that defines a size of a next descriptor in a descriptor list.

6. (Original) A DMA controller as defined in claim 1, wherein a size of a first DMA descriptor is defined by a register value.

7. (Original) A DMA controller as defined in claim 1, wherein a size of the DMA descriptor is defined by a previous descriptor.

8-9. (Cancelled)

10. (Original) A DMA controller as defined in claim 5, wherein the channel control logic is configured to fetch elements of a next descriptor in response to the next descriptor size.

11. (Original) A DMA controller as defined in claim 10, wherein the channel control logic is configured to decrement a descriptor element count from the next descriptor size during fetching of descriptor elements.

12. (Original) A DMA controller as defined in claim 1, wherein the channel control logic is configured to fetch programmable descriptors in a list of descriptors.

13. (Original) A DMA controller as defined in claim 12, wherein the descriptors in the list of descriptors have different formats.

14. (Original) A DMA controller as defined in claim 12, wherein the descriptors in the list of descriptors have different sizes.

15. (Currently amended) A method for DMA transfer, comprising:

providing a DMA datapath for transferring data from a DMA source to a DMA destination; and

controlling transfer of data through the DMA datapath in response to parameters contained in at least one DMA descriptor having a programmable format, wherein each DMA descriptor defines a single DMA transfer, wherein the DMA descriptor includes a next descriptor pointer that points to a next descriptor in a descriptor list, wherein the next descriptor pointer is selected from (1) none, which indicates descriptor array mode, (2) half of the next descriptor pointer, which indicates small descriptor list mode, and (3) all of the next descriptor pointer, which indicates large descriptor list mode, and wherein the DMA descriptor further includes a flow mode that defines a next operation selected from an autobuffer mode, the descriptor array mode, the small descriptor list mode and the large descriptor list mode.

16. (Original) A method as defined in claim 15, further comprising fetching a next descriptor based on information contained in a current descriptor.